



香港中文大學

The Chinese University of Hong Kong

CENG3430 Rapid Prototyping of Digital Systems
Lecture 00: Course Information

Ming-Chang YANG

mcyang@cse.cuhk.edu.hk



CENG3430 Course Information



- **CENG3430 Rapid Prototyping of Digital Systems**

- **Course Time and Place (Online!)**

- **Lecture (*2)**

- MON 16:30~18:15 ([ZOOM](#) @ ~~LSB LT6~~)

- **Lab (*2)**

- TUE 16:30~18:15 ([ZOOM](#) @ ~~SHB 102~~)

- Note: You're required to attend both lab sessions.



zoom

The recordings
will be available
at Blackboard.

- **Course Website**

- <http://www.cse.cuhk.edu.hk/~mcyang/ceng3430/2021S/ceng3430.html>
- <https://blackboard.cuhk.edu.hk/>

Course Instructor & Teaching Assistants

- **Course Instructor**

- Prof. Ming-Chang YANG (楊明昌)

- Office: SHB 906 (3943-8405)
- Office Hours: *Requested by email*
- Email: mcyang@cse.cuhk.edu.hk

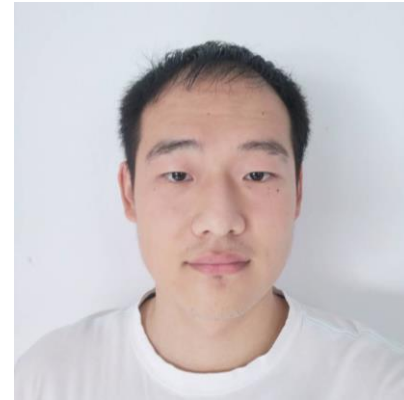
- **Teaching Assistants**

- Chao WANG (王超)

- Office: SHB 921
- Office Hours: WED 16:00~17:00 ([ZOOM](#))
- Email: cwang@cse.cuhk.edu.hk

- Lok Yin CHOW (周樂言)

- Office: SHB 921
- Office Hours: THU 11:30~12:30 ([ZOOM](#))
- Email: lychow@cse.cuhk.edu.hk



Course Assessment



- **Grading** (*subject to changes*)
 - ~~Class Exercises~~ ~~0%~~ (cancelled!)
 - Weekly Lab Exercises 40%
 - Final Project 40%
 - Final Exam 20%
 - Bonus 5% (be active!)
- **Notes**
 - Weekly Lab Exercises: Individual
 - Final project: At most two students in a group
 - Late submission is **NOT** acceptable (unless otherwise approved before the regular deadline)

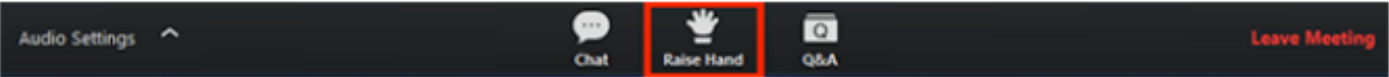
Questions? Raise Hand or Chat



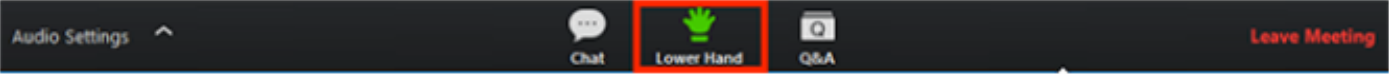
- To have good quality of online classes, I will **mute everyone** by default.
- Questions? [Raise Hand](#)

Windows | Mac

1. Click **Raise Hand** in the Webinar Controls.



2. The host will be notified that you've raised your hand.
3. Click **Lower Hand** to lower it if needed.



- Questions? [In-meeting Chat](#)



We Are Surrounded by Digital Systems

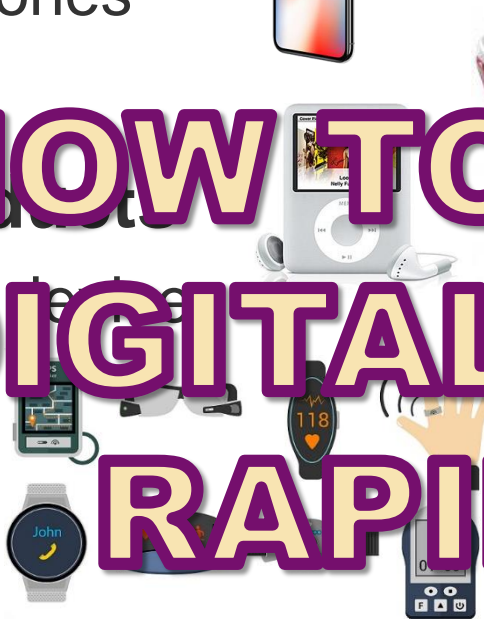
- **Mass Products**

- Media players
- Mobile phones



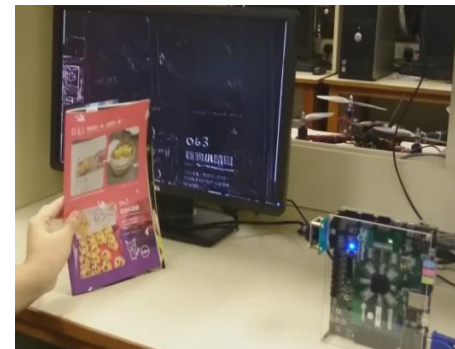
- **Novel Products**

- Wearable devices
- Robots



- **Research**

- Real time edge detection
- Deep learning acceleration



**HOW TO BUILD
A DIGITAL SYSTEM
RAPIDLY?**



Common Design Flow of Digital System



Idea Generation

Drafting on Paper

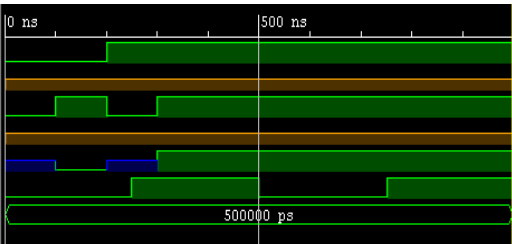
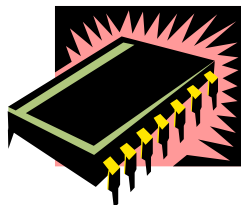
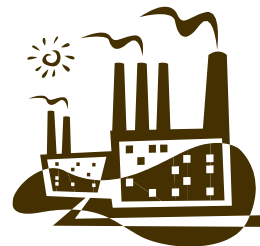
Designing Chip (VHDL)

Testing (FPGA)

Manufacturing
Production Line Design

Quality Control

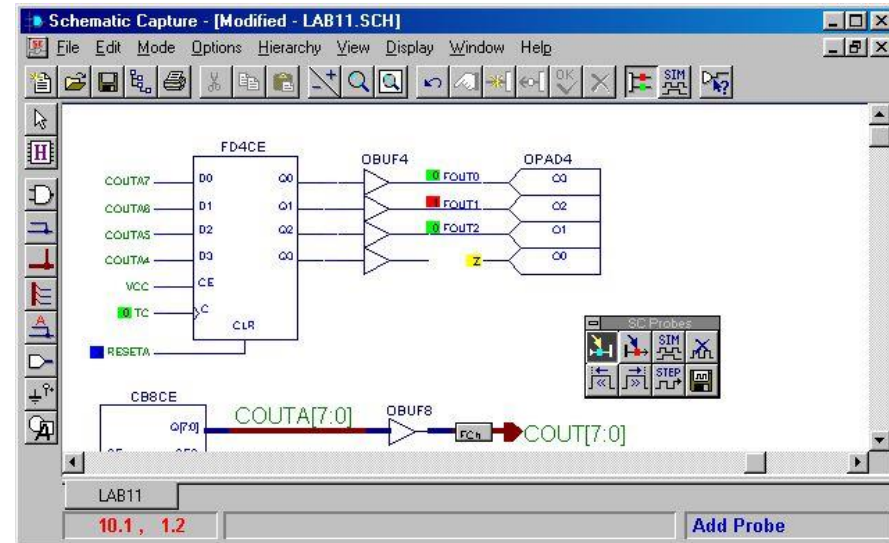
```
Ex: VHDL AND-Gate Program
1 entity and2 is
2 port (a,b: in std_logic;
3       c: out std_logic);
4 end and2
5 architecture arch of and2
6 begin
7     c <= a and b;
8 end and2_arch
```



Methods for Digital System Design



- **Schematic Method**
 - **Complicated**
 - Suitable for **top level design** to merge **modules**
 - Like data flow block diagram



- **Programming Language**

- **VHDL** (Very-High-Speed-Integrated-Circuits Hardware Description Language)
 - Each **module** in the schematic can be implemented by VHDL.
- **Verilog**

Ex: VHDL AND-Gate Program

```
1 entity and2 is
2 port (a,b: in std_logic;
3       c: out std_logic);
4 end and2
5 architecture and2_arch of and2
6 begin
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8 end and2_arch
```


Our Focus: Prototyping



Idea Generation

Drafting on Paper

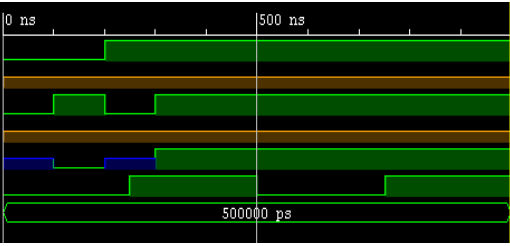
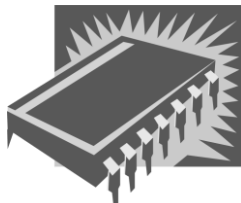
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What We Will Learn

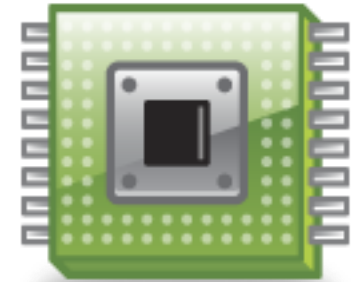


- **Software: Hardware Description Language (HDL)**

Ex: VHDL AND-Gate Program

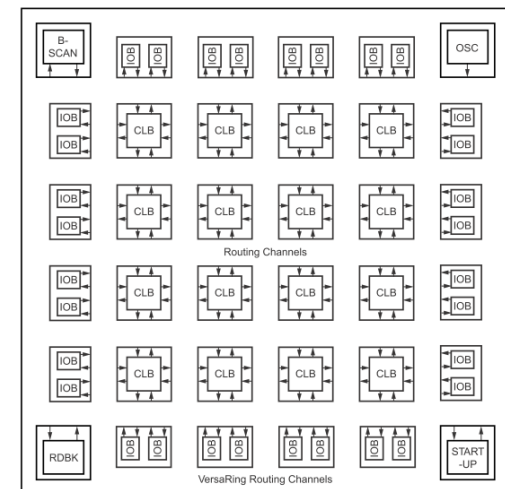
```
1 entity and2 is
2 port (a,b: in std_logic;
3       c: out std_logic);
4 end and2
5 architecture and2_arch of and2
6 begin
7     c <= a and b;
8 end and2_arch
```

*Write HDL code,
then it will generate
the hardware chip
automatically*



- **Hardware: Field Programmable Gate Array (FPGA)**

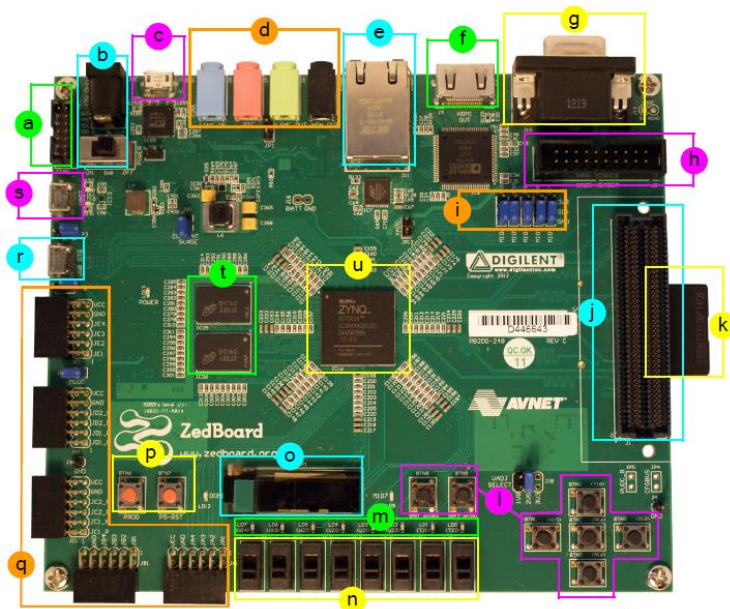
- The hardware can be **reprogrammable**.
- Designs can be changed **easily**.
- No additional hardware manufacturing **cost** is needed.



What We Will Use in Our Lab



- **Software:** Vivado WebPACK™ Edition (**FREE**)
 - It supports **Windows** or **Linux** operating systems.
 - **Hardware Description Language:** Very-High-Speed-Integrated-Circuits Hardware Description Language (**VHDL**)
- **Hardware:** Zynq ZedBoard
 - Dual-core ARM Cortex-A9 with traditional FPGA



- | | | |
|---------------------------------|--------------------------------|------------------------------------|
| a Xilinx JTAG connector | h XADC header port | o OLED display |
| b Power input and switch | i Configuration jumpers | p Prog & reset push buttons |
| c USB-JTAG (programming) | j FMC connector | q 5 x Pmod connector ports |
| d Audio ports | k SD card (underside) | r USB-OTG peripheral port |
| e Ethernet port | l User push buttons | s USB-UART port |
| f HDMI port (output) | m LEDs | t DDR3 memory |
| g VGA port | n Switches | u Zynq device (+ heatsink) |

Software: Vivado WebPACK™ Edition



example - [E:/example/example.xpr] - Vivado 2016.3

File Edit Flow Tools Window Layout View Help

Flow Navigator

- Project Manager
 - Project Settings
 - Add Sources
 - Language Templates
 - IP Catalog
- IP Integrator
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- Simulation
 - Simulation Settings
 - Run Simulation
- RTL Analysis
 - Elaboration Settings
 - Open Elaborated Design
- Synthesis
 - Synthesis Settings
 - Run Synthesis
 - Open Synthesized Design
- Implementation
 - Implementation Settings
 - Run Implementation
 - Open Implemented Design
- Program and Debug
 - Bitstream Settings
 - Generate Bitstream
 - Open Hardware Manager

Project Manager example

Sources

Messages: 1 warning

- Design Sources (1)
 - example - example_arch (example.vhd)
- Constraints
- Simulation Sources (1)

Hierarchy Libraries Compile Order

Source File Properties

example.vhd

Enabled

Location: E:/example/example.srcs/sources_1/new

Type: VHDL

Library: xil_defaultlib

Size: 0.6 KB

General Properties

Design Runs

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	PCIe %	Start	Elapsed	Strateg
synth_1	constrs_1	Not started															Vivado
impl_1	constrs_1	Not started															Vivado

Tcl Console Messages Log Reports Design Runs

Project Summary example.vhd

Project Settings

Project name: example

Project location: E:/example

Product family: Zynq-7000

Project part: ZedBoard Zynq Evaluation and Development Kit (xc7z020clg484-1)

Top module name: example

Target language: VHDL

Simulator language: Mixed

Board Part

Display name: ZedBoard Zynq Evaluation and Development Kit

Board part name: em.avnet.com.zed.part01.3

Repository path: C:/Xilinx/Vivado/2016.3/data/boards/board_files

URL: <http://www.zedboard.org>

Board overview: ZedBoard Zynq Evaluation and Development Kit

Synthesis

Status: Not started

Messages: No errors or warnings

Implementation

Status: Not started

Messages: No errors or warnings

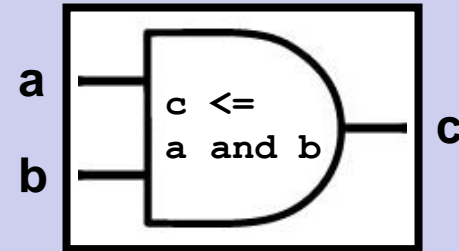
Hardware Description Language: VHDL

- **An Example: AND-Gate in VHDL**

Entity Declaration: Define I/Os

```
1 entity and2 is
2   port (a,b: in std_logic;
3         c: out std_logic);
4 end and2
```

```
5 architecture and2_arch of and2
6 begin
7   c <= a and b;
8 end and2_arch
```

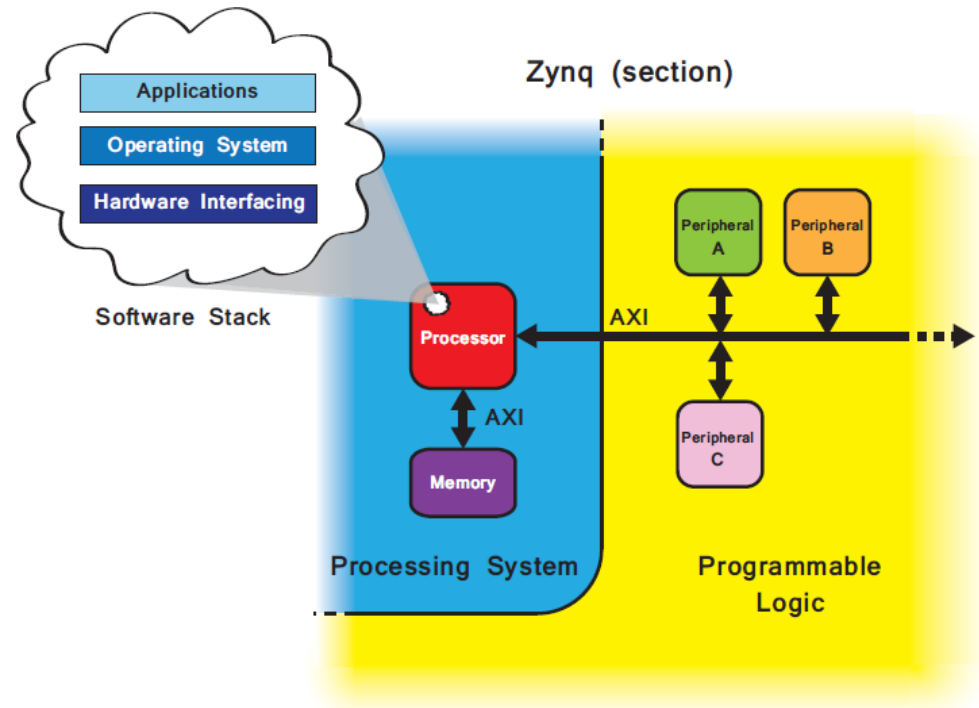
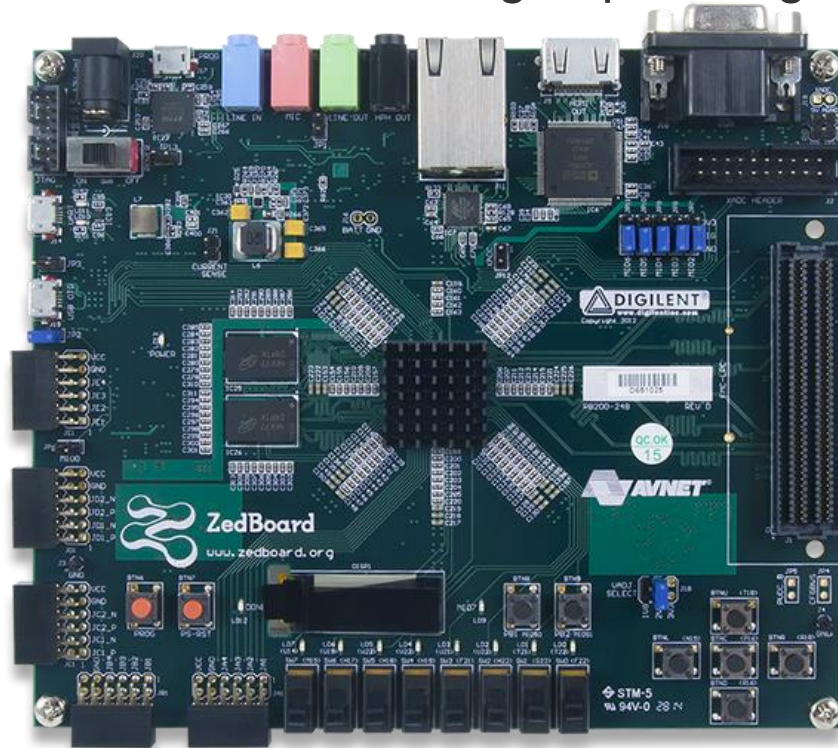


Architecture Body: Define functions

Hardware: Zynq ZedBoard



- Zynq ZedBoard combines
 - **Processing System (PS):** Dual-core ARM Cortex-A9 CPU
 - Supports software routines and/or operating systems
 - **Programmable Logical (PL):** Equivalent to trad. FPGA
 - Ideal for high-speed logic, arithmetic and data flow subsystems



Course Schedule



W	Date	Lecture	Lab
1	Jan 11, 12	Lec00: Course Information	No Lab
2	Jan 18, 19	Lec01: Introduction to VHDL	Lab01: Vivado & Software Simulation
3	Jan 25, 26	Lec02: Introduction to ZedBoard	Lab02: First Program on ZedBoard
4	Feb 1, 2	Lec03: Architectural Styles of VHDL	Lab03: 4-to-1 Multiplexer
5	Feb 8, 9	Lec04: Comb. Circuit and Seq. Circuit	Lab04: Serial-in-parallel-out Shift Register
6	Feb 15, 16	Lunar New Year Vacation (No Class)	Lunar New Year Vacation (No Lab)
7	Feb 22, 23	Lec05: Driving Clock and Pmod	Lab05: Driving Seven Segment Display
8	Mar 1, 2	Lec06: Driving VGA Display	Lab06: Driving VGA Display
9	Mar 8, 9	Lec07: Integration of ARM and FPGA	Lab07: Software Stopwatch
10	Mar 15, 16	Lec08: Embedded Operating System	Lab08: Software Stopwatch with Linux
11	Mar 22, 23	Final Project Proposal	Final Project Proposal Feedback
12	Mar 29, 30	Reading Week (No Class)	Reading Week (No Lab)
13	Apr 5, 6	Public Holiday (No Class)	Public Holiday (No Lab)
14	Apr 12, 13	Lec09: High Level Synthesis	Lab09: High Level Synthesis Exercise
15	Apr 19, 20	Lec10: Introduction to Verilog	Lab10: Verilog Exercise
	May 9	Final Project Submission Deadline	



- **Equipment**

- Every student will get a full set of hardware equipment for practice by local mail ~~or picking up at SHB 102~~.
- We cannot ship lab materials to oversea students.

- **Attendance and Guidance**

- During regular lab sessions, students conduct lab exercises online and can reach out instructor/TAs for online help.
- TAs will host two additional 60-minute online help sessions weekly during their office hours.
- The breakout room of Zoom will be used to provide students individual assistance and guidance.

- **Submission and Demonstration**

- Students need to tap and upload short demo videos.

Full Final Project List (2019-20)



1. AVG Game
2. [Door Locking System](#)
3. [The Flappy Bird](#)
4. Immigration System
5. [Traffic Horn Punishment](#)
6. [How Fast Is Your Finger](#)
7. [Mastermind](#)
8. [Drum Looper](#)
9. [Gobang](#)
10. [Morse Code from Torch](#)
11. [Indoor Monitoring Station](#)
12. [Rhythm Game](#)
13. [Cat Dog Fight Game](#)
14. [Portable Freezer](#)
15. [Color Detector](#)
16. [Mastermind](#)
17. [Tic Tac Toe](#)
18. [UFO Catcher](#)
19. Sound Recorder



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Full Final Project List (2018-19)



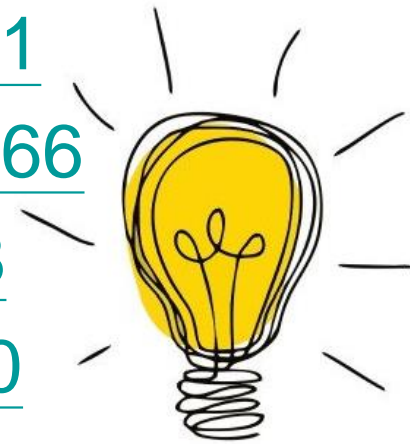
1. [Piano and Music Player](#)
2. [Color Recognition](#)
3. [RGB Meter](#)
4. [Lie Detector](#)
5. [Snake Battle](#)
6. [Space War](#)
7. [The Dodge Game](#)
8. [Space Impact](#)
9. [Get It at Once](#)
10. [Elevator](#)
11. [Super Pads](#)
12. [Tetris](#)
13. [Morse Code Interpreter](#)
14. [The Flash](#)
15. [Multifunctional Display](#)
16. [Rolling Down!](#)



WOW IDEA

Selective Final Projects (17-18 & 16-17)

- Piano: https://youtu.be/_VH3fUazEEI?t=87
- Music Player: <https://youtu.be/dEdnp1Tni9c?t=27>
- Bullhorn: <https://youtu.be/dtQ88yL0FUM?t=26>
- Wash Machine: <https://youtu.be/z7C8dXn9EQ0?t=10>
- Thermometer: <https://youtu.be/i0swDnATRt4?t=41>
- Space Invader: <https://youtu.be/2wEG-U8DNak?t=72>
- Tetris: <https://youtu.be/JyEU1YbYMrc?t=11>
- Snake: <https://youtu.be/dFdr0KqXw7Q?t=66>
- Car: <https://youtu.be/FDbSyYKHYes?t=28>
- Sonar: <https://youtu.be/DiLjDbkbejs?t=180>

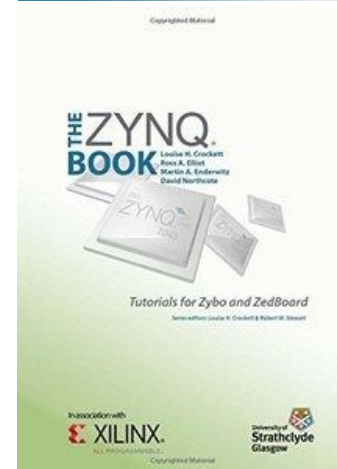
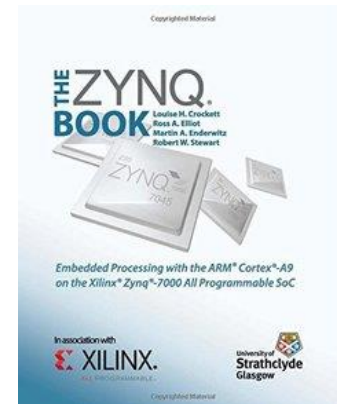
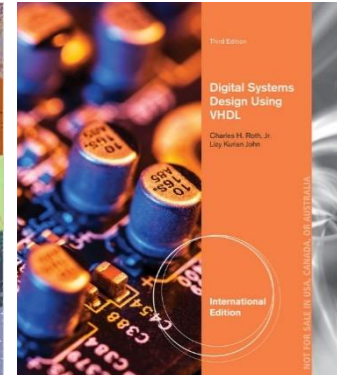
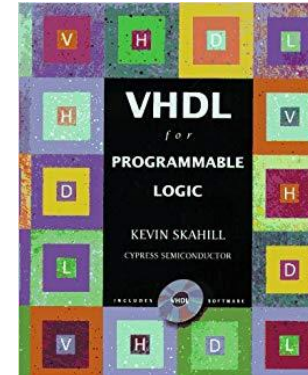


WOW IDEA

References



- **VHDL for Programmable Logic**
 - Kevin Skahill
 - Addison-Wesley
- **Digital Systems Design Using VHDL**
 - Charles H. Roth Jr., Lizy Kurian John
 - Cengage Learning
- **The Zynq Book: Embedded Processing with the Arm Cortex-A9 on the Xilinx Zynq-7000 All Programmable Soc**
 - Louise H Crockett, Ross A Elliot, Martin A Enderwitz, Robert W Stewart
 - Strathclyde Academic Media
- **The Zynq Book: Tutorials for Zybo and ZedBoard**
 - Louise H Crockett, Ross A Elliot, Martin A Enderwitz
 - Strathclyde Academic Media



Important Notes



- Visit our course website regularly!
- Plagiarism will **NOT** be tolerated!
 - Don't copy!
 - Don't let other(s) copy!
 - Can discuss but write up the solutions by yourself!
- Honesty in Academic Work:
 - <http://www.cuhk.edu.hk/policy/academichonesty/>

The best way to learn is through practice!

Severe Penalties on Dishonesty (1/3)

(iii)	<p>Employing or using services provided by a third party [Note 1] to undertake the examinations/ final year projects/ papers/ essays/ dissertations, or providing services as a third party, including any one of the following aspects:</p> <p>(a) employing or using services provided by a third party;</p> <p>(b) providing services as a third party;</p> <p>(c). sharing of any materials obtained from the employment or use of services provided by a third party to other students; and</p> <p>(d) knowingly using materials obtained by anyone who has employed or used the services provided by a third party.</p>	(i)	three demerits (of which one will remain in the University's record permanently and two are reviewable);
		(ii)	a failure grade for the course concerned (not applicable to the student who is the third party to provide the services but not taking the same course or not taking it in the same term);
		(iii)	suspension from the University for one term [Note 2]; and
		(iv)	lowering the degree classification by one level upon graduation (not applicable to undergraduate students who graduate with a Pass Degree, MBChB students and postgraduate students) [Note 3].
(v)	<p>Distribution/ Sharing/ Copying of teaching materials without the consent of the course teachers to gain unfair academic advantage in the courses</p>	(i)	two demerits.

Severe Penalties on Dishonesty (2/3)

(vi)	<p>Violating rule 15 or 16 of the University's Examination Rules (Annex 1) or rule 9 or 10 of the University's Online Examination Rules (Annex 2)</p>	<p><u>First offence</u></p> <p>(i) one demerit.</p> <p><u>Second or further offence (and a first offence that is serious as decided by the disciplinary committee concerned/the FTP Committee)</u></p> <p>(i) two demerits (of which one will remain in the University's record permanently and one is reviewable).</p>
(vii)	<p>Cheating in tests and examinations (including violation of rule 17 or 18 of the University's Examination Rules or rule 11, 12, 13, 14 or 16 of the University's Online Examination Rules)</p>	<p><u>First offence</u></p> <p>(i) one demerit (which will remain in the University's record permanently); and</p> <p>(ii) a failure grade for the course concerned.</p> <p><u>Second or further offence (and a first offence that is serious as decided by the disciplinary committee concerned/the FTP Committee)</u></p> <p>(i) two demerits (of which one will remain in the University's record permanently and one is reviewable); and</p> <p>(ii) a failure grade for the course concerned.</p>

Severe Penalties on Dishonesty (3/3)

(viii)	Impersonation fraud in tests and examinations (including violation of rule 19 of the University's Examination Rules or rule 15 of the University's Online Examination Rules)	(i)	three demerits (of which one will remain in the University's record permanently and two are reviewable);
		(ii)	a failure grade for the course concerned;
		(iii)	suspension from the University for one term [Note 1]; and
		(iv)	lowering the degree classification by one level upon graduation (not applicable to undergraduate students who graduate with a Pass Degree, MBChB students and postgraduate students) [Note 2].
		[The same penalties apply to the student who asks/allows someone to assume his/her identity to sit for a test/an examination as well as to the student who sits for a test/an examination if both parties are students of the University, except that penalty (ii) will not apply to the latter.]	